REMARKS

Claims 1-20 are pending. Claims 9, 13-16, and 18 have been amended. Claim 12 has been cancelled without prejudice. No new matter has been added. It is asked that all claims be allowed in view of the amendment to the claims above and the remarks below.

Objections to the Drawings:

The drawings stand objected to for various informalities. The drawings have been amended to show every feature of the claimed invention and to include proper labels. No new matter has been added. Withdrawal of the objections to the drawings in view of the current amendments is respectfully requested.

Objections to the Specification:

The specification stands objected to for the reasons addressed below. The title of the invention has been amended to more clearly indicate the invention to which the claims are directed. The abstract has been amended to comply with MPEP § 608.01(b). No new matter has been added by these amendments.

The specification stands objected to for failing to include a summary section. This objection is respectfully traversed. The cited rule states what a specification should include, and falls short of making a summary section mandatory. Intel Corporation has taken the position that they prefer to omit summaries in their applications. Since compliance with Rules 73 and 77 is entirely voluntary, it is respectfully suggested that the application is totally complete without a summary section, and therefore the requirement for a summary section is respectfully traversed.

Objections to, and 112 rejections of, claims 9 and 15-20:

Claims 9 and 18 stand objected to for specified informalities. These claims have been amended to correct these informalities, and thus, withdrawal of the objections are respectfully requested.

Claims 15-20 stand rejected under 35 U.S.C. 112, second paragraph as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. The stated interpretation of claims 15 and 16 is correct, and these claims have been amended accordingly. In view of this, withdrawal of the 112 rejection of claims 15-20 is respectfully requested.

Rejection of claims 1, 2, 4, and 6-8:

Claims 1, 2, 4, and 6-8 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Levitan (EP 0605872 A1). This contention is respectfully traversed. Levitan is directed to preservation of non-conditional state information for recovery after speculative execution fails. In Levitan, a dispatch version register 42 provides a dispatch stage version of the count to be used for address generation. A completion version register 46 holds the count corresponding to the last speculatively executed and confirmed instruction, and an update version register 44 holds the count for an instruction speculatively executed, which will be copied into the completion version register 46 when confirmed, thus enabling decrementing of the dispatch version count in register 42 before a MOVE_TO_COUNT instruction completes execution, as the MOVE_TO_COUNT instruction may itself be speculatively executed. (See col. 6, lines 29-54.)

During operation, the contents of a general purpose register 40 are copied into registers 42 and 44 upon execution of a MOVE_TO_COUNT instruction, and dispatch register 42 is decremented upon dispatch of a BRANCH_ON_COUNT instruction. If an interrupt is taken prior to completion of instructions following a BRANCH_ON_COUNT instruction, then the contents of completion register 46 are copied into dispatch register 42, which returns the state of dispatch register 42 to that preceding execution of any speculative instructions not yet confirmed. Moreover, the contents of update register 44 are copied to completion register 46 with completion of the MOVE_TO_COUNT instruction, and completion register 46 is decremented upon removal of the tentative markings from the results of the branch. (See col. 7, lines 2-46.) Thus, even if the value in the completion register 46 can be considered to be an adjustment value as claimed, Levitan still only teaches calculation of a single adjustment value.

In contrast, independent claim 1 recites "calculating adjustment values at stages within a pipeline of the processor", which by its plain meaning calls for multiple adjustment values to be calculated in multiple stages (e.g., a separate adjustment value being calculated at each execution stage of a pipeline as described in the specification). Levitan fails to teach or suggest calculation of multiple adjustment values at multiple stages within a pipeline of a processor, as claimed. Claims 2, 4, and 6-8 each depend from independent claim 1, and thus all of claims 1, 2, 4, and 6-8 are patentable over Levitan for at least this reason.

Moreover, with respect to claim 6, Levitan never discusses watch points. The official action states that, "In order to detect each instruction, it is inherent that a watch point must

exist for it, and thus this watch point is detected for each instruction." However, watch points are neither described nor necessary in Levitan for detecting instructions. Detection of the relevant branch instructions in Levitan is easily accomplished using the processor hardware itself, which is by necessity able to identify all instruction types that conform to its instruction set architecture. The claimed technique involving detection of a watch point, as that term is understood in the art and defined in the specification at page 9, lines 7-16, is in no way inherent in the teachings of Levitan.

With respect to claim 7, it should first be noted that termination of an instruction, as claimed, is in fact very different than completion of an instruction; the official action suggests that they are equivalent. Completion of an instruction involves execution and then retirement of the instruction, whereas termination of an instruction involves canceling the instruction before retirement. Second, decrementing of the completion register 46, in Levitan, upon instruction completion does not constitute "adjusting the register by an amount determined by a counter residing in the stage where the termination occurred", as claimed. This is made clear by the rejection of claim 1 in the official action, where the value in register 46 and the dispatch register 42 of Levitan are equated with the claimed "adjustment values" and "register", respectively, and yet in the rejection of claim 7, the value in register 46 and then register 46 itself are equated with the claimed "adjustment value" and "register", respectively. Thus, the stated reasons for the rejections of claims 1 and 7 do not appear to be self consistent.

Moreover, a key limitation in claim 7, "adjusting the register by an amount determined by a counter residing in the

stage where the termination occurred", is not shown in Levitan. There is no indication in Levitan that a stage in which a termination occurs is ever determined. Thus, for all of the above reasons, withdrawal of the rejection of claims 1, 2, 4, and 6-8 is respectfully requested, and it is respectfully suggested that these claims should be allowable.

Rejection of claims 9-13 and 15:

Claims 9-13 and 15 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Gaertner (5,996,063). This contention is respectfully traversed. Independent claim 9 has been amended to include all the limitations of original dependent claim 12, and claims 13-15 have been amended to depend from claim 9 instead of claim 12. Claim 12 has been cancelled.

Gaertner is directed to a register renaming and allocation scheme in superscalar computer systems in which the architected registers (those registers that hold the in-order state of the processor) are made part of the temporary register arrays, thus avoiding the need to transfer values in temporary register storage to architected registers. A register allocator in Gaertner includes counters that keep track of which temporary storage registers currently hold the in-order state of the processor, and which temporary registers hold temporary out-of-order values (i.e., which of the temporary registers currently hold renamed register values), if any. The I0/I1 counter values identify which registers hold the in-order state, the R0/R1 counter values identify the latest rename instance in the registers, and the U0/U1 counter values indicate how many rename instances exist by tracking the difference between the counters R0/R1 and I0/I1. (See col. 13, lines 4-50.)

All of these counters, I0/I1, R0/R1 and U0/U1, reside in the same stage of the processor: the register renaming and allocation stage. The official action itself acknowledges this fact in paragraph 28: "the register renaming and allocation block where the set of counters resides, as described above, is the fifth stage." Thus, Gaertner neither teaches nor suggests "the set of counters include counters maintained at a stage where the first register resides and at stages after the stage where the first register resides", as claimed. Therefore, claims 9-11, 13 and 15 are patentable over Gaertner for at least this reason.

With respect to claims 13 and 15 in particular, because Gaertner does not teach counters in multiple stages in a multi-stage pipeline, as claimed, the use of Gaertner to further reject claims 13 and 15 under 35 U.S.C. 102(b) cannot be supported. For example, Gaertner does not anticipate claim 15 because Gaertner does not include a control unit that decrements "a respective counter when an instruction associated with the condition leaves a respective stage associated with the respective counter."

Additionally, with respect to claims 10 and 11, while the I0/I1 counters are registers that identify the architected registers, they are not themselves architected registers as suggested. The I0/I1 counters merely loop through the binary numbers 00 to 11 in order to identify the registers in the processor that currently hold the in-order state of the processor. Moreover, it is important to note that out-of-order execution in a processor is not equivalent to speculative execution, as suggested in the official action. Out-of-order execution involves dispatching instructions to the functional units out of their sequential program order, and speculative

execution involves predicting the outcome of a branch in a program before the branch instruction has been resolved and fetching instructions, which may never be completely executed in the case of a branch mis-prediction, based on the speculative branch prediction. A processor architecture need not include both out-of-order execution and speculative execution together. Thus, the fact that a processor performs register renaming to support out-of-order execution, such as described in Gaertner, does not imply that the processor performs speculative execution or that renamed temporary registers can be considered speculative registers as claimed. For all of these reasons, it is respectfully suggested that claims 9-13 and 15 should be allowable.

Rejections of claims 3, 5, 14, 16-17, and 20:

Claim 3 stands rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Levitan in view of Gschwing (6,189,088). Claim 5 stands rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Levitan in view of Tran (6,003,128). These contentions are respectfully traversed. For the reasons discussed above, Levitan does not anticipate claim 1. Claims 3 and 5 each depend from claim 1, and neither Gschwing nor Tran cure the deficiency of Levitan. Thus, claims 3 and 5 are patentable over the suggested combination of Levitan and Gschwing for at least this reason.

Claim 14 stands rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Gaertner in view of Levitan. This contention is respectfully traversed. Claim 14 now depends from amended claim 9, and for the reasons discussed above, Gaertner does not anticipate amended claim 9. Additionally, for reasons discussed above in connection with claims 1 and 7,

Levitan neither teaches nor suggests: "following a termination of an instruction in the pipeline, the control unit is adapted to adjust the first register by an amount determined by a particular counter maintained in a stage where the termination occurred", as recited in claim 14. Gaertner does not cure this deficiency in Levitan. Therefore, claim 14 is patentable over the suggested combination of Gaertner and Levitan for at least these reasons.

Claims 16-17 and 20 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Levitan in view of Hennessy. Claims 18 and 19 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Levitan in view of Hennessy, and in further view of Nakada (5,638,526). These contentions are respectfully traversed. For the reasons discussed above, Levitan neither teaches nor suggests the claimed control unit of claims 16-20, and neither Hennessy nor Nakada cure these defects in Levitan. Thus, claims 16-20 are patentable over the suggested combinations of Levitan, Hennessy and Nakada for at least these reasons.

In view of the above amendments and remarks, multiple aspects of patentable novelty and non-obviousness, which the claims present, have been clearly identified in view of the state of the art disclosed by the cited references, the rejections, and the objections made. It has been shown how the amendments avoid the cited references and why the rejections and objections should be withdrawn. Thus, in view of the above amendments and remarks, all of the claims should be in condition for allowance. A formal notice of allowance is thus respectfully requested.

In addition, it is believed that all of the pending claims have been addressed. However, the absence of a reply to a

specific issue or comment does not signify agreement with or concession of that issue or comment. Because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Enclosed is a $110 check for the Petition for Extension of Time fee. Please apply any other necessary charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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